Single phase inverter circuit diagram

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Single Phase Inverter is an electrical circuit, converts a fixed voltage DC to a fixed (or variable) single phase AC voltage with variable frequency. A single Phase Inverter can be used to control the speed of single-phase motors.

Consider Q, Q, QB and Q as IGBTs. The above Fig. 3.6 (a) shows single phase bridge inverter with RL load. The construct is same as that of single phase bridge inverter with resistive load. And the diodes DI, D2, DB and D4 are the feedback elements.

At time t ti the pair of transistors QI and Q2 is turned ON. The transistors act as a closed switch and hence ‘A’ gets connected to positive terminal of the dc source. ‘B’ gets connected to the negative terminal of the input supply or dc source.

The load current starts increasing exponentially due to the inductive nature of the load. The instantaneous current through QI and Q2 is equal to the instantaneous load current through RL The energy is stored into the inductive load during this interval (i.e. tl -- t2).

At time t --t3, the transistor Q3 and Q4 are turned ON simultaneously. The output load voltage remains negative equal to (--V) volts but the direction of load current will reverse and its magnitude becomes negative. The current increases in the negative direction and energy is stored in the load. This operation is shown in the following (3.6)

The mode IV operation is same as that in mode I. At instant t4 (to) the transistors QB and are turned OFF. The load inductance tries to maintain the load current in the same direction by inducting a positive load voltage. Due to which the diodes DI and D2 are forward biased, and thus the energy stored in the load inductance is returned back to the input dc supply. The value of load voltage Vo = +V, but the load current remains negative and decreases to zero. The operation in this interval is shown in Fig. 3.6 (f).

Thus, the square wave output voltage contains odd harmonics. Here, in single pulse modulation (SPM), the output pulse delay in the beginning while it is advanced at the end by equal interval of(Tt -- ?)/2 shown in following Fig. 3.8 (b).

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